IN THE SPECIFICATION:

Please replace paragraph [0026] with the following amended paragraph:

[0026] FIG. 1 illustrates an exemplary DDR DRAM device 100 utilizing a "return clock" signal in accordance with embodiments of the present invention. The DDR DRAM device 100 generally includes a plurality of memory arrays 102 and various control logic 104, such as a command decoder 106, used to interpret externally supplied commands to access (e.g., read, write, or refresh) data stored in the memory arrays 102. As illustrated, data to be read from the memory arrays 102 may be driven by drivers 130 to a read data latch 132, via an internal bus [[131]]181, and then placed onto an external data bus (labeled DQ[0:N]) from a data out register 107. Similarly, data to be stored in the memory arrays 102 may be latched from the external data bus into a data-in register 108. From the data-in register 108, the data may be written to the memory arrays 102 by driving the data onto an internal data bus 116, via write driver circuits 112 of an I/O gating 110. The internal data bus 116 is coupled to receivers 118 which latches the incoming data. The internal data bus 116 may also be referred to as an "on-chip" bus since this bus is an element of the DDR DRAM device 100 which couples other elements resident on the DDR DRAM device 100. This may be contrasted to the external data bus, DQ[0:N], which couples the DDR DRAM device 100 to some other external device, e.g., a controller.